WHAT IS CLAIMED IS:

1. A process of transforming an original netlist for an integrated circuit to a final netlist employing only universal gates having four inputs and two outputs, the universal gate being arranged to perform at least two logic functions, the process comprising steps of:

a) input an original netlist in basic form of two-input gates and inverters, each gate and inverter having an output;

b) creating a negation net for each net coupled to an input or output of each gate and to an input of each inverter;

c) removing each gate of the original netlist and inserting a universal gate in its stead such that the nets previously coupled to the inputs and output of the removed gate and a negation of those nets are coupled to the inputs and outputs of the inserted universal gate in a selected arrangement; and

d) removing each inverter of the original netlist and negating the net previously coupled to the input of the inverter.

2. The process of claim 1, wherein the original netlist contains first gates performing an anding function and second gates performing an oring function, each first and second gate having inputs a,b and outputs z coupled to respective nets U1,U2,U3, in the form of (.a(U1),.b(U2),.z(U3)), and

wherein performance of step b creates respective negation nets U1_neg,U2_neg,U3_neg, wherein step c includes:

removing each first gate from the original netlist and inserting a universal gate in the form (.a1(U1),.b1(U2),.z1(U3),.a2(U1_neg),.b2(U2_neg), .z2(U3_neg)) its stead, and

removing each second gate from the original netlist and inserting a universal gate in the form (.a1(U1_neg),.b1(U2_neg),.z1(U3_neg),.a2(U1),.b2(U2), .z2(U3)) its stead.

3. The process of claim 2, wherein the first gates are NAND gates and the second gates are NOR gates.

4. The process of claim 2, wherein the original netlist includes inverters having inputs a and outputs z coupled to respective nets U4,U5, in the form (.a(U1),.z(U2)), wherein step d includes:

removing each inverter from the original netlist and assigning U5=U4_neg and U5_neg=U4.

5. The process of claim 4, wherein the first gates are NAND gates and the second gates are NOR gates.

6. The process of claim 4, further including:

e) creating a final netlist based on the results of steps c and d.

7. The process of claim 1, further including:

e) creating a final netlist based on the results of steps c and d.

8. A universal gate for an integrated circuit comprising:

a first gate performing an anding function having first and second inputs providing a first output; and

a second gate performing an oring function having third and fourth inputs providing a second output,

the first, second, third and fourth inputs being arranged for selective coupling to respective first and second nets and negations of the first and second nets, and the first and second outputs being arranged for selective coupling to a third net and a negation of the third net.

9. The universal gate of claim 8, wherein the universal gate replaces a netlist representation of a two-input gate coupled to the first and second nets to perform an anding function, the universal gate being arranged so that the first and second inputs are coupled to the first and second nets, respectively, the third and fourth inputs are coupled

to the negations of the first and second nets, respectively, and the first and second outputs are coupled to the third net and the negation of the third net, respectively.

10. The universal gate of claim 8, wherein the universal gate replaces a netlist representation of a two-input gate coupled to the first and second nets to perform an oring function, the universal gate being arranged so that the first and second inputs are coupled to the negations of the first and second nets, respectively, the third and fourth inputs are coupled to the first and second nets, respectively, and the first and second outputs are coupled to the negation of the third net and the third net, respectively.

11. The universal gate of claim 8, wherein the first gate is defined as $F(x\_1,\ldots,x\_n)$ and the second gate is defined as $G(x\_1,\ldots,x\_n)$, where $G(x\_1,\ldots,x\_n) = \sim F(\sim x\_1,\ldots,\sim x\_n)$.

12. The universal gate of claim 8, wherein the first gate is a NAND gate and the second gate is a NOR gate.

13. An integrated circuit composed of universal gates according to claim 8.

14. The integrated circuit of claim 13, characterized by an absence of inverters.

15. A computer useable medium having a computer readable program embodied therein for addressing data to transform an original netlist containing two-input gates and inverters for an integrated circuit to a final netlist employing only universal gates having four inputs and two outputs, the universal gate being arranged to perform at least two logic functions, the computer readable program comprising:

first computer readable code for causing the computer to create a negation net for each net coupled to an input or output of each gate and to an input of each inverter;

second computer readable code for causing the computer to remove each gate of the original netlist and inserting a universal gate in its stead such that the nets coupled to the inputs and output of the removed gate and a negation of those nets are coupled to the inputs and outputs of the inserted universal gate in a selected arrangement; and

third computer readable code for causing the computer to remove each inverter of the original netlist and negate the net coupled to the input of the inverter.

16. The computer useable medium of claim 15, wherein the original netlist contains first gates

performing an anding function and second gates performing an oring function having inputs a,b and outputs z coupled to respective nets U1,U2,U3, in the form of (.a(U1),.b(U2),.z(U3)), and wherein execution of the first computer readable code creates respective negation nets U1_neg,U2_neg,U3_neg, wherein the second computer readable code includes:

computer readable code for causing the computer to remove each first gate from the original netlist and insert a universal gate in the form (.a1(U1),.b1(U2),.z1(U3),.a2(U1_neg),.b2(U2_neg), .z2(U3_neg)) its stead, and

computer readable code for causing the computer to remove each second gate from the original netlist and insert a universal gate in the form (.a1(U1_neg),.b1(U2_neg),.z1(U3_neg),.a2(U1),.b2(U2), .z2(U3)) its stead.

17. The computer useable medium of claim 16, wherein the original netlist includes inverters having inputs a and outputs z coupled to respective nets U4,U5, in the form (.a(U1),.z(U2)), wherein the third computer readable code includes:

computer readable code for causing the computer to remove each inverter from the original netlist and assign U5=U4_neg and U5_neg=U4.

18. The computer useable medium of claim 17, wherein the first gates are NAND gates and the second gates are NOR gates.

19. The computer useable medium of claim 16, wherein the first gates are NAND gates and the second gates are NOR gates.

20. The computer useable medium of claim 15, further including:

computer readable code for causing the computer to create a final netlist based on the results of execution of the second and third computer readable codes.